

REMARKS

Claims 1-90 are currently pending in this Application, with claims 23-54 and 59-85 having been previously withdrawn. Claim 88 has been amended.

No new matter has been introduced by these amendments. Reconsideration and allowance of the claims are respectfully requested in view of the above amendments and the following remarks.

Objection to the Claims

Claim 86 has been objected to. In response, Applicant respectfully withdraws claim 86.

Claim Rejections Under 35 U.S.C. §102

Claims 1-6, 9, 10, 12-22, 55-58, and 87-90 are rejected as being anticipated under 35 U.S.C. 102(b) by Wunner, U.S. Patent No. 6,674,332 (hereinafter "Wunner"). Applicant respectfully traverses.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Applicant's claim 1 recites, *inter alia*,

"*attenuating jitter* of said input timing reference (TR) to produce a control signal...at least one of said intermediate clock signals (IC) being *justified* to a local clock (LC) and being *spectrum controlled*."

Applicant first notes that *justification* or "*being justified*" is commonly known in the art of telecommunications to refer to an asynchronous process. For example, the "ATIS Telecom Glossary 2000," (www.atis.org/tg2k/) defines justification as "The process the digit rate of a digital signal in a controlled manner so that it is in accord with a digit rate different from its own inherent rate, usually without loss of information," and the "Fiber Optics Standard Dictionary"

(<http://books.google.co.uk/books?id=s56JS2WkXE4C>) defines justification as “The movement and alignment of data with respect to a fixed reference, such as a clock or frame alignment signal.” Further, in sections 2, 3, and 4 of the book titled “synchronization of Digital Telecommunications Networks” (<http://books.google.co.uk/books?id=APEBaL4WHNoV>), justification is further discussed as follows,

“In asynchronous digital multiplexers, bit synchronization of tributary signals into the multiplex signal is performed by means of a bit justification (historically known as pulse stuffing or bit stuffing[...]. The specification bit is often omitted but helps to distinguish from the pointer justification technique, adopted in SDH and SONET, which is sometimes also referred to as byte justification.

The term ‘justification’ originated in the printing industry, where it describes the process of adjusting the spaces between printed words so that all the lines of print have the same length. Another practical example of justification is embodied in the concept of leap year. A nominal length calendar year is 365 days long, but to make the calendar year nearly the same as the solar year an extra day is added to the year at the end of February approximately once every four years.”

Accordingly, as is evidenced by the above definitions and discussion, “justification” is an asynchronous process as opposed to a synchronous process.

Wunner does not teach at least one of the intermediate clock signals (IC) being *justified* to a local clock (LC), as justification is discussed and defined above. Instead of teaching a justification, Wunner teaches use of a local clock (pullable crystal 242) as an intermediate clock signal, wherein the local clock is tweaked so that the phase of the local clock is forced to approach the phase of the input timing reference. In other words, Wunner teaches a synchronizing, which, as is discussed in the definitions and passages above, is the opposite of the justification (or “being justified”) recited in Applicant’s claim 1. Thus, Applicant respectfully asserts that Wunner does not teach intermediate clock signals (IC) being *justified* to a local clock (LC), as would be required for anticipation.

Furthermore, the asynchronicity of the above discussed justification leads to jitter. Wunner does not teach or suggest introduced jitter or attenuation of said jitter, nor does Wunner

teach spectrum control. Instead, referring to column 7 lines 31-36, Wunner teaches an adjustment of frequency of the crystal 242. This may change the intermediate signal from containing one single frequency to another single frequency, but does not teach spectrum control over all frequencies as the recited justification of the intermediate clock signal (to a local clock) and recited jitter attenuation of the timing reference and intermediate clock signal entails.

With more specific reference to dependent claim 3, Applicant points out that there is recited a justification and spectrum control that is numerical. Similarly, claims 5, 56 and 57 mention use of a number controlled oscillator, and claim 17 mentions the intermediate clock being established by a numeric stage. Applicant respectfully traverses the Examiner's assertion that the analog embodiment of Figure 4 of Wunner discloses a numerical control, or is a numeric stage. At column 7 line 23 of Wunner there is mentioned the voltage of control signal 216" and in column 7 line 31 is mentioned that the oscillator circuit 232" that may be a voltage controlled crystal oscillator [VCXO]. Voltage control and analog circuits are typically not considered numerical, if not explicitly stated and provided for. Thus, in addition to Wunner not disclosing justification and spectrum control at all (see above), Applicant additionally and respectfully asserts that the processes the Examiner equates with justification and spectrum control are not numerical.

With more specific reference to dependent claim 4, Applicant respectfully traverses the Examiner's finding of low-pass filtering or attenuation of jitter being taught in Wunner. While Wunner discloses a loop-filter, there is nothing taught in Wunner of the filter's configuration. Thus, Applicant respectfully asserts that Wunner does not teach the low-pass filtering of claim 4.

With more specific reference to dependent claim 6, Applicant respectfully points out that the Examiner does not address or suggest any element taught in Wunner that would be an equivalent of Applicant's claimed period control input. As taught at paragraph [0226] of the Applicant's US publication, and figures 3A and 3B, an oscillator with frequency control has a linear relationship between control input and output frequency, meaning that a reciprocal relationship exists between control input and the output *period*. Therefore the period control entails a linear relationship between the control input and the output period, allowing a reciprocal

relationship between the control input and the output frequency. In other words, higher *frequency control* values mean higher frequency, and higher *period control* values mean longer periods, i.e., lower frequency. The Wunner circuit uses frequency control, as the control voltage controls the frequency of the oscillator. Period control is, respectfully, not taught by Wunner.

With more specific reference to dependent claim 12, there is recited a first loop being a time locked loop. Applicant respectfully points out that the Examiner equates the loop of Figure 4 of Wunner with the time locked loop recited in Applicant's claim 12. However, Applicant respectfully asserts that the Wunner circuit is a phase locked loop using phase detectors and stating proportional relationships between phase difference and control signal. Thus the Wunner loop is not a time locked loop.

Accordingly, Applicants respectfully submit that for at least the reasons set forth hereinabove, Claims 1-6, 9, 10, 12-22, 55-58, and 87-90 are not anticipated by Wunner. Reconsideration and allowance of Claims 1-6, 9, 10, 12-22, 55-58, and 87-90 are respectfully requested.

Claims 1 and 11 are rejected as being anticipated under 35 U.S.C. 102(b) by Wang, U.S. Patent No. 6,094,569 (hereinafter "Wang"). Applicant respectfully traverses.

Applicant's claim 1 recites *inter alia*,

"attenuating jitter of said input timing reference (TR) to produce a control signal; providing at least one intermediate clock signal (IC) on a basis of said control signal, at least one of said intermediate clock signals (IC) being justified to a *local clock (LC)* and being spectrum controlled."

Applicant first notes that Wang does not teach any local clock input (to allow the intermediate clock signals to be justified to the local clock) to any of the voltage controlled oscillators (VCO) of Wang. Instead, Wang teaches the output of VCO1 to be justified to the output of VCO2. In other words, Wang teaches the output of a phase locked loop to be justified

to one of its inputs. Applicant respectfully asserts that such a teaching is not equatable to an intermediate clock signals (IC) being justified to a local clock (LC). Furthermore, Applicant respectfully points out that the output of the Wang circuit is not taught to be the output of VCO2 (as the Examiner suggests at page 7 of the Office Action), but is instead the output of VCO1. Still further, Wang teaches nothing of “being justified” (as justification is defined with reference to Wunner above), jitter, jitter attenuation, or spectrum control.

Accordingly, Applicants respectfully submit that for at least the reasons set forth hereinabove, Claims 1 and 11 are not anticipated by Wang. Reconsideration and allowance of Claims 1 and 11 are respectfully requested.

Claim Rejections Under 35 U.S.C. §103

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being obvious over Wunner. Applicant respectfully traverses.

To establish a *prima facie* case of obviousness, it is known that three basic criteria must be met: (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art reference(s) must teach or suggest all the claim limitations. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d 1016, 1023 (Fed. Cir. 1996).

Dependent claims inherit all of the limitations of the parent claim. Claims 7 and 8 depend from Claim 1. As discussed above, Wunner does not disclose all of the elements recited in amended Claim 1. Thus, *prima facie* obviousness does not exist regarding Claims 7 and 8 with respect to Wunner.

Additionally, since Wunner fails to teach or suggest all of the limitations of Claims 7 and 8, clearly, one of ordinary skill at the time of Applicant’s invention would not have a motivation

to modify the reference, nor a reasonable likelihood of success in forming the claimed invention by modifying the reference. Thus, here again, *prima facie* obviousness does not exist.

Accordingly, Applicants respectfully submit that for at least the reasons set forth hereinabove, Claims 7 and 8 are not obvious Wunner. Reconsideration and allowance of Claims 7 and 8 are respectfully requested.

Conclusion

All of the objections and rejections are herein overcome. In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. No new matter is added by way of the present Amendments and Remarks, as support is found throughout the original filed specification, claims and drawings. Prompt issuance of Notice of Allowance is respectfully requested.

The Examiner is invited to contact Applicants' attorney at the below listed phone number regarding this response or otherwise concerning the present application.

Applicants hereby petition for any necessary extension of time required under 37 C.F.R. 1.136(a) or 1.136(b) which may be required for entry and consideration of the present Reply.

If there are any charges due with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130 maintained by Applicants' attorneys.

Respectfully submitted,

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